CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A method for fabricating packaged integrated circuit dies in a wafer format, said method comprising:

providing a wafer substrate, said wafer substrate having a top surface and a bottom surface;

fabricating a plurality of integrated circuits on the top surface of the wafer substrate, each of the integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate relative to the integrated circuits;

depositing top-side bond pads on the top surface of the substrate in contact with the signal vias, said top-side pads being in electrical contact with an integrated circuit;

depositing back-side bond pads on the bottom surface of the substrate in contact with the signal vias to make an electrical connection between the top-side pads and the back-side pads;

depositing a top-side protective layer on the wafer substrate to cover the top-side pads and the integrated circuits;

removing portions of the substrate material in the scribe lanes from the bottom of the substrate between the integrated circuits;

depositing a back-side protective layer on the wafer substrate so that the

back-side layer fills the removed portions of the substrate in the scribe lanes and contacts the top-side protective layer;

forming signal vias through the back-side layer to be in electrical contact with the back-side bond pads; and

cutting the wafer substrate in the scribe lanes to separate the wafer into the packaged dies so that an outer surface of the packaged dies includes exposed signal vias to make electrical connections thereto.

2. (Original) The method according to claim 1 further comprising forming a plurality of ground vias extending through the substrate in electrical contact with a back metal layer of the integrated circuits.

3. (Original) The method according to claim 2 further comprising depositing a ground plane on the bottom surface of the substrate adjacent to the back-side pads in electrical contact with the ground vias.

4. (Original) The method according to claim 3 further comprising forming ground vias through the back-side layer in electrical contact with the ground plane.

5. (Original) The method according to claim 1 wherein removing portions of the substrate material includes removing portions of the substrate material between signal vias outside of the scribe lanes.

6. (Original) The method according to claim 1 wherein removing portions of the substrate material includes preventing substrate material of the wafer substrate beneath the integrated circuits from being removed.

7. (Original) The method according to claim 1 further comprising testing the integrated circuits for performance prior to cutting the wafer.

8. (Original) The method according to claim 1 further comprising forming vias through the top-side protective layer that are in electrical contact with the top-side pads.

9. (Original) The method according to claim 8 further comprising stacking a plurality of the packaged dies where the vias through the back-side layer in one die are in electrical contact with the vias through the top-side layer in another die.

10. (Original) The method according to claim 1 wherein the top-side layer and the back-side protective layer include plastic layers.

11. (Currently Amended) A method for fabricating a packaged integrated circuit die, said method comprising:

providing a wafer substrate, said wafer substrate having a first surface and a second surface;

fabricating integrated circuits on the first surface of the wafer substrate,

each of the integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate, said signal vias being electrically coupled to the integrated circuits;

enclosing the integrated circuits in a protective layer;

forming signal vias through the protective layer that are electrically coupled to the signal vias formed through the substrate; ~~and~~

cutting the wafer substrate in the scribe lanes to separate the wafer into packaged dies where the signal vias in the substrate and the protective layer are exposed[[.]] ; and

forming ground vias extending through the substrate in electrical contact with a back metal of an integrated circuit.

12. (Currently Amended) The method according to claim 11 wherein ~~forming~~ enclosing the integrated circuits in a protective layer includes forming a first protective layer in contact with the first surface of the wafer substrate and forming a second protective layer in contact with the second surface of the wafer substrate, wherein the first protective layer and the second protective layer are in contact with each other in the scribe lanes.

13. (Original) The method according to claim 11 further comprising etching the wafer substrate to remove wafer substrate material in the scribe lanes.

14. (Original) The method according to claim 11 further comprising

depositing a plurality of first side bond pads on the first surface of the substrate in electrical contact with the signal vias in the substrate and in electrical contact with an integrated circuit, and depositing a plurality of second side bond pads on the second surface of the substrate in electrical contact with the signal vias in the protective layer.

15. Cancelled.

16. (Currently Amended) The method according to claim 11 [[15]] further comprising depositing a ground plane on the second surface of the substrate in electrical contact with the ground vias in the substrate.

17. (Currently Amended) The method according to claim 11 [[15]] further comprising forming ground vias through the protective layer in electrical contact with the ground plane.

18. (Currently Amended) The method according to claim 11 further comprising testing the integrated circuit chips for performance prior to cutting the wafer substrate.

19. (Original) A method for fabricating packaged integrated circuit dies in a wafer format, said method comprising:

providing a wafer substrate, said wafer substrate having a top surface and a bottom surface;

fabricating a plurality of integrated circuits on the top surface of the wafer substrate, said integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate relative to the integrated circuits;

depositing top-side bond pads on the top surface of the substrate in electrical contact with the signal vias, said top-side pads being in electrical contact with an integrated circuit;

depositing back-side bond pads on the bottom surface of the substrate in electrical contact with the signal vias to make an electrical connection between the top-side pads and the back-side pads;

forming a plurality of ground vias extending through the substrate in electrical contact with a back metal layer of the integrated circuits;

depositing a ground plane on the bottom surface of the substrate adjacent to the back-side pad in electrical contact with the ground vias;

forming ground vias through the back-side layer in electrical contact with the ground plane;

depositing a top-side protective layer on the wafer substrate to cover the top-side pads and the integrated circuits;

removing portions of the substrate material in the scribe lanes, wherein removing portions of the substrate material includes removing portions of the substrate material between signal vias outside of the scribe lanes and preventing substrate material of the wafer substrate beneath the integrated circuits from being removed from the bottom of the substrate between the integrated circuits;

depositing a back-side protective layer on the wafer substrate so that the

back-side layer fills the removed portions of the substrate in the scribe lanes and contacts the top-side protective layer;

forming signal vias through the back-side layer to be in electrical contact with the back-side bond pads; and

cutting the wafer substrate in the scribe lanes to separate the wafer into the packaged dies so that an outer surface of the packaged dies includes exposed signal vias to make electrical connections thereto.

20. (Original) The method according to claim 19 further comprising forming vias through the top-side protective layer that are in electrical contact with the top-side pads, and stacking a plurality of the packaged dies where the vias to the back-side layer in one die are in electrical contact with the vias through the top-side layer in another die.

21. (New) A method for fabricating a packaged integrated circuit die, said method comprising:

providing a wafer substrate, said wafer substrate having a first surface and a second surface;

fabricating integrated circuits on the first surface of the wafer substrate, each of the integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate, said signal vias being electrically coupled to the integrated circuits;

enclosing the integrated circuits in a protective layer including forming a first protective layer in contact with the first surface of the wafer substrate and forming a

second protective layer in contact with a second surface of the wafer substrate, wherein the first protective layer and the second protective layer are in contact with each other in the scribe lanes;

forming signal vias through the protective layer that are electrically coupled to the signal vias formed through the substrate; and

cutting the wafer substrate in the scribe lanes to separate the wafer into packaged dies where the signal vias in the substrate and the protective layer are exposed.

22. (New) A method for fabricating a packaged integrated circuit die, said method comprising:

providing a wafer substrate, said wafer substrate having a first surface and a second surface;

fabricating integrated circuits on the first surface of the wafer substrate, each of the integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate, said signal vias being electrically coupled to the integrated circuits;

enclosing the integrated circuits in a protective layer;

forming signal vias through the protective layer that are electrically coupled to the signal vias formed through the substrate;

cutting the wafer substrate in the scribe lanes to separate the wafer into packaged dies where the signal vias in the substrate and the protective layer are exposed; and

etching the wafer substrate to remove wafer substrate material in the scribe lanes.

23. (New) A method for fabricating a packaged integrated circuit die, said method comprising:

providing a wafer substrate, said wafer substrate having a first surface and a second surface;

fabricating integrated circuits on the first surface of the wafer substrate, each of the integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate, said signal vias being electrically coupled to the integrated circuits;

enclosing the integrated circuits in a protective layer;

forming signal vias through the protective layer that are electrically coupled to the signal vias formed through the substrate;

cutting the wafer substrate in the scribe lanes to separate the wafer into packaged dies where the signal vias in the substrate and the protective layer are exposed; and

depositing a plurality of first side bond pads on the first surface of the substrate in electrical contact with the signal vias in the substrate and in electrical contact with an integrated circuit, and depositing a plurality of second side bond pads on the second surface of the substrate in electrical contact with the signal vias in the protective layer.

24. (New) A method for fabricating a packaged integrated circuit die, said method comprising:

providing a wafer substrate, said wafer substrate having a first surface and a second surface;

fabricating integrated circuits on the first surface of the wafer substrate, each of the integrated circuits being separated from each other by scribe lanes;

forming signal vias through the substrate, said signal vias being electrically coupled to the integrated circuits;

enclosing the integrated circuits in a protective layer;

forming signal vias through the protective layer that are electrically coupled to the signal vias formed through the substrate;

cutting the wafer substrate in the scribe lanes to separate the wafer into packaged dies where the signal vias in the substrate and the protective layer are exposed; and

testing the integrated circuit chips for performance prior to cutting the wafer substrate.